Demonstrate seven different logic functions

NXP demo board for the configurable logic device 74AUP1T97

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Key features and benefits

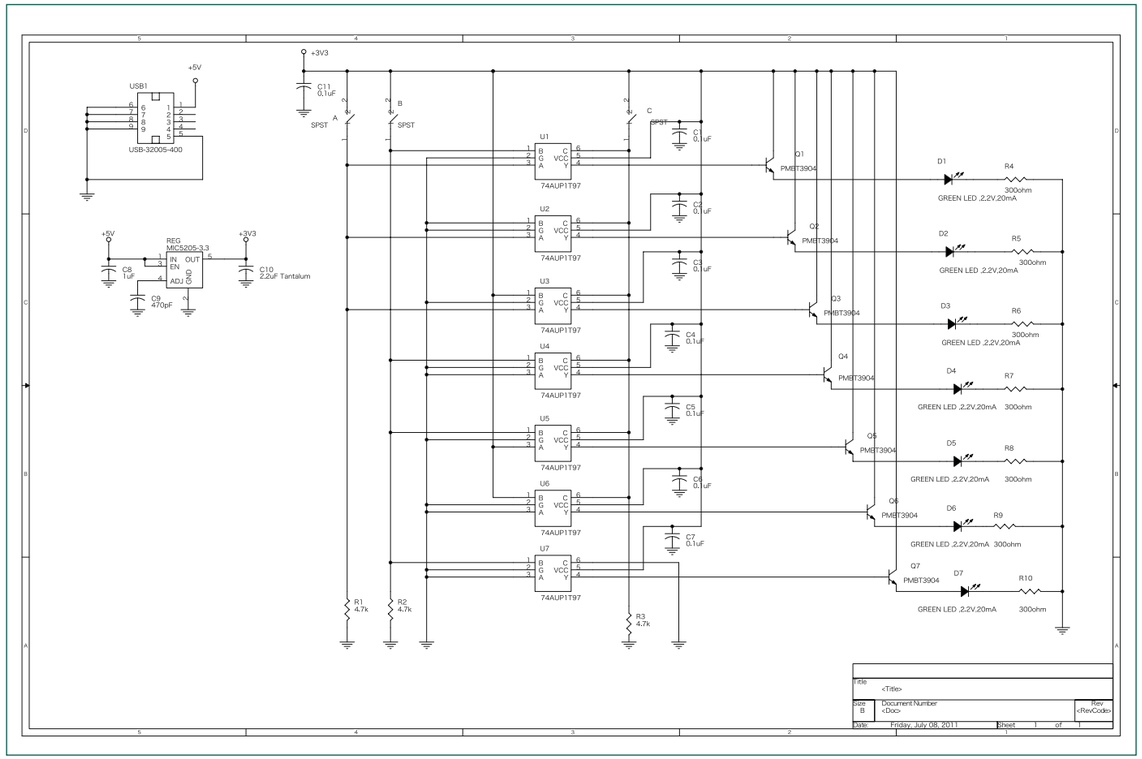
- Wide supply voltage range: 2.3 to 3.6 V
- High noise immunity
- Excellent ESD protection
  - HBM JESD22-A114F Class 3A exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption: I_{CC} = 1.5 µA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low-noise over- and undershoot <10% of V_{CC}
- IOFF circuitry provides operation in partial power-down mode
- Multiple package options
- Specified from -40 to +85 and -40 to +125 °C

The 74AUP1T97 provides low-power, low-voltage configurable logic gate functions. The output state is determined by eight patterns of a three-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, or buffer. All inputs can be connected to V_{CC} or GND. The device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 2.3 to 3.6 V.

The device is designed for logic-level translation applications with input switching levels that accept low-voltage (1.8 V) CMOS signals while operating from a single supply voltage of 2.5 or 3.3 V. The wide supply voltage range ensures normal operation as battery voltage drops from 3.6 to 2.3 V. The device is fully specified for partial power-down applications using IOFF, which disables the output and thus prevents the device from damaging backflow current when powered down. Schmitt trigger inputs make the circuit tolerant to slower input rise and fall times across the entire V_{CC} range.

A circuit schematic of the 74AUP1T97 demo board is given below. The board includes seven 74AUP1T97 devices, each configured for a different logic function. Each device has an identical "Y" output circuit, which includes a green LED (2.2 V, 20 mA), an NPN drive transistor, and a current limiting resistor. Three toggle switches, used with input pins A, B, and C, are marked on the schematic. A Mini-USB socket provides supply power through a 3.3 V fixed output regulator to the circuit. The USB data lines are not connected and USB control is not available.

Circuit schematic of 74AUP1T97 demo board



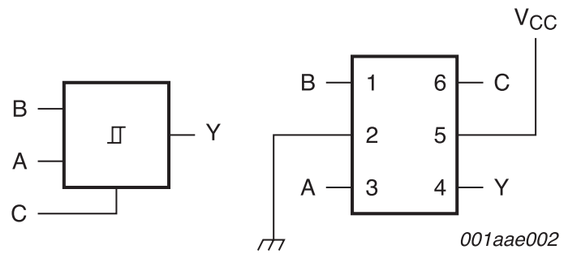
Operating instructions for demo board

Using a standard-to-mini-USB cable (not included), connect the USB power source (a power supply or a PC USB socket) to the demo board's Mini-USB socket. With the NXP logo on the top right side of the board and the three toggle switches closest to the user, the input LO position is to the left and the input HI position is to the right. Devices U1 thru U6 are located from left to right across the board Changing the positions of the A, B, and C switches will demonstrate that each 74AUP1T97 device is configured to implement a different logic function, as indicated by the LEDs.

Operation of device U1 (far left side of board)

U1 is configured as a two-input MUX. Switch C selects either an A or B input level and transfers the signal to output Y. The truth table is shown below.

A	B	C	Y	D1
0	0	0	0	Off
1	0	0	0	Off
1	1	0	0	On
0	1	0	0	On
1	0	1	1	On
1	1	1	1	On
0	1	1	0	Off

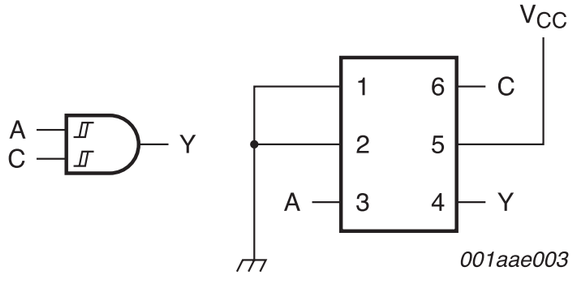


Operation of device U2 (second from left)

U2 is configured as a two-input AND gate. Toggle switches A and C to demonstrate the function. Note that LED D2 lights up only when A and C inputs are held high. The truth table is shown below.

A	B	C	Y	D2
0	0	0	0	Off
1	0	0	0	Off
1	1	0	0	Off
0	1	0	0	Off
1	0	1	1	On
1	1	1	1	On
0	1	1	0	Off

* Note that toggling the B switch has no impact on the AND gate function since the B input is hardwired to GND in this case.

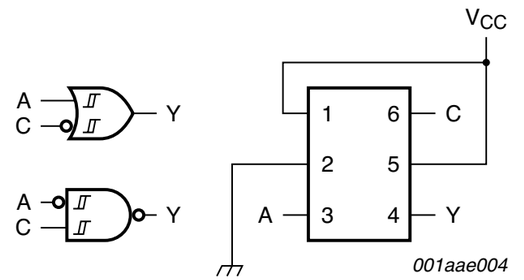


Operation of device U3 (3rd from left)

U3 is configured as a two-input OR gate with an inverted C input. Toggle switches A and C to demonstrate the function. Note that LED D' lights up except when A = 0 and C is 1. The truth table is shown below.

A	B	C	Y	D3
0	0	0	1	On
1	0	0	1	On
1	1	0	1	On
0	1	0	1	On
1	0	1	1	On
1	1	1	1	On
0	1	1	0	Off

* Note that toggling the B switch has no impact on the gate function since the B input is hardwired to V_{cc} in this case.

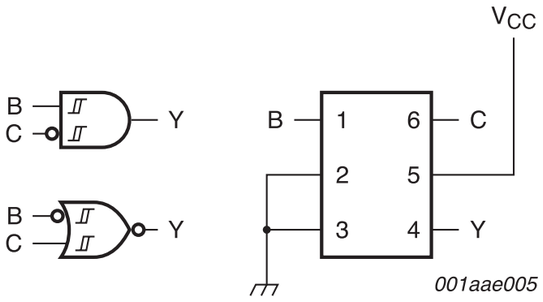


Operation of device U4 (center)

U4 is configured as a two-input AND gate with an inverted C input. Toggle switches B and C to demonstrate the function. Note that LED D4 stays off except when B = 1 and C is 0. The truth table is shown below

A	B	C	Y	D4
0	0	0	0	Off
1	0	0	0	Off
1	1	0	1	On
0	1	0	1	On
1	0	1	1	Off
1	1	1	0	Off
0	1	1	0	Off

* Note that toggling the A switch has no impact on the gate function since the A input is hardwired to GND in this case.

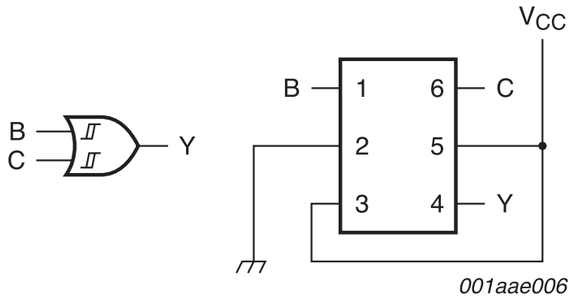


Operation of device U5 (third from right)

U5 is configured as a two-input OR gate. Toggle switches B and C to demonstrate the function. Note that LED D5 stays on as long as either or both of the B and C inputs are 1. The truth table is shown below.

A	B	C	Y	D5
0	0	0	0	Off
1	0	0	1	On
1	1	0	1	On
0	1	0	1	On
1	0	1	0	Off
1	1	1	0	Off
0	1	1	1	On

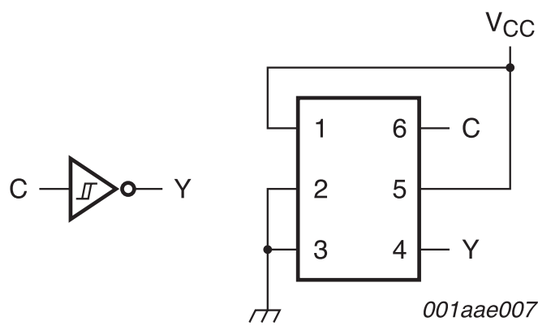
* Note that toggling the A switch has no impact on the gate function since the A input is hardwired to V_{cc} in this case.



Operation of device U6 (second from right)

U6 is configured as a single channel inverter. Toggle switch C to demonstrate the function. Note that LED D6 stays on as long as the C input/switch is 0 (held low). The truth table is shown below.

A	B	C	Y	D6
0	0	0	1	On
1	0	0	1	On
1	1	0	1	On
0	1	0	1	On
1	0	1	0	Off
1	1	1	0	Off
0	1	1	0	Off

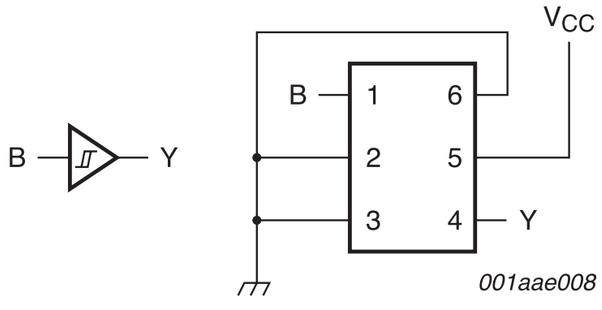


* Note that toggling the A and B switches has no impact on the inverter function since the A input is hardwired to GND and the B input is hardwired to V_{cc} in this case.

Operation of device U7 (far right)

U7 is configured as a single channel buffer. Toggle switch B to demonstrate the function. Note that LED D7 stays on as long as the B input/switch is 1 (held high). The truth table is shown below.

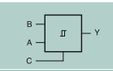
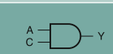
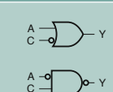
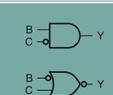
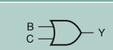
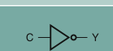
A	B	C	Y	D7
0	0	0	0	Off
1	0	0	0	Off
1	1	0	1	On
0	1	0	1	On
1	0	1	0	Off
1	1	1	1	On
0	1	1	1	On



* Note that toggling the A and C switches has no impact on the buffer function since the A and C inputs are hardwired to GND in this case.

User Reference Card

This card is sized to fit on the back of the demo board. Print it, cut it out and fasten it to the back of the board as a handy reference.

2-input MUX C selects A, B	
2-input AND A, C input	
2-input OR A, inverted C input 2-input NAND C, Inverted A input	
2-input AND B, inverted C input 2-input NOR C, inverted B input	
2-input OR B, C input	
Invert C	
Buffer B	

Packages

The 74AUP1T97 is available in the following 6-pin packages: SOT363, SOT886, SOT891, SOT1115, SOT1202

Package Suffix	GW	GM	GF	GN	GS
					
Width (mm)	1.9	1.3	1.0	0.9	1.0
Length (mm)	1.2	1.0	1.0	1.0	1.0
Height (mm)	0.95	0.5	0.5	0.35	0.35
Pitch (mm)	0.65	0.5	0.35	0.30	0.35

Ordering Information

Part Number	Package				
	Temp. range	Name	Type	Marking	Material
74AUP1T97GW	-40 to 125 °C	SC-88	Surface-mounted package	59	Plastic
74AUP1T97GM	-40 to 125 °C	XSON6	Extremely thin small outline package; no leads	59	Plastic
74AUP1T97GF	-40 to 125 °C	XSON6	Extremely thin small outline package; no leads	59	Plastic
74AUP1T97GN	-40 to 125 °C	XSON6	Extremely thin small outline package; no leads	59	Plastic
74AUP1T97GS	-40 to 125 °C	XSON6	Extremely thin small outline package; no leads	59	Plastic

Other configurable logic devices

The NXP portfolio includes more than a dozen configurable logic devices, covering the most common logic functions.

Part	Translator	True Schmitt Trigger inputs	AND	AND both inverted inputs	AND one inverted input	Buffer	Inverter	MUX	MUX with inverted output	NAND	NAND both inverted inputs	NAND one inverted input	NOR	NOR both inverted inputs	NOR one inverted input	OR	OR both inverted input	OR one inverted input	XNOR	XOR
74AUP1G57		√	√	√		√	√					√	√	√				√	√	
74AUP1T57*	√	√	√	√		√	√					√	√	√				√	√	
74LVC1G57		√	√	√		√	√					√	√	√				√	√	
74AUP1G58		√			√	√	√			√	√				√	√	√			√
74AUP1T58*	√	√			√	√	√			√	√				√	√	√			√
74LVC1G58		√			√	√	√			√	√				√	√	√			√
74AUP1G97		√	√		√	√	√	√				√			√	√		√		
74AUP1T97*	√	√	√		√	√	√	√				√			√	√		√		
74LVC1G97		√	√		√	√	√	√				√			√	√		√		
74AUP1G98		√			√	√	√		√	√		√	√		√			√		
74AUP1T98*	√	√			√	√	√		√	√		√	√		√			√		
74LVC1G98		√			√	√	√		√	√		√	√		√			√		
74LVC1G99		√	√	√	√	√	√	√	√	√	√	√							√	√

Package options for other configurable logic devices

The table below lists the SOT number and the corresponding NXP package suffix for each configurable logic device.

Part	363 GW	457 GV	833 GT	886 GM	891 GF	902 GM	996 GD	1089 GF	1115 GN	1116 GN	1202 GS	1203 GS
74AUP1G57	√			√	√				√		√	
74AUP1T57*	√			√	√				√		√	
74LVC1G57	√	√		√	√				√		√	
74AUP1G58	√			√	√				√		√	
74AUP1T58*	√			√	√				√		√	
74LVC1G58	√	√		√	√				√		√	
74AUP1G97	√			√	√				√		√	
74AUP1T97*	√			√	√				√		√	
74LVC1G97	√	√		√	√				√		√	
74AUP1G98	√			√	√				√		√	
74AUP1T98*	√			√	√				√		√	
74LVC1G98	√	√		√	√				√		√	
74LVC1G99			√			√	√	√		√		√

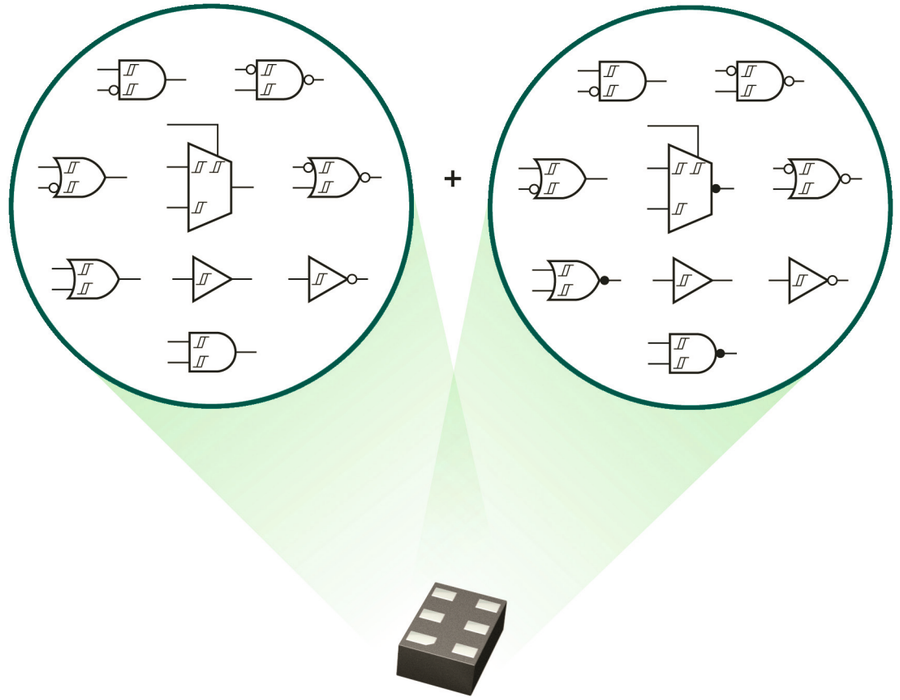
* 74AUP1TXX functions have lower input switching thresholds than 74AUP1GXX devices. The 74AUP1TXX versions can also be used in logic-level translation applications, where input switching levels accept low-voltage (1.8 V) CMOS signals while operating from a single supply voltage of 2.5 or 3.3 V.

Other configurable logic devices

The NXP portfolio includes more than a dozen configurable logic devices, covering the most common logic functions.

Configurable Logic offers:

- **Flexibility** by integrating 9 different functions including non standard logic functions in a single device
- **Cost saving** by reducing the number of devices in inventory
- **Space savings** by reducing the need for two devices on PCB. Also, the voltage level translation is integrated that eliminates the need of additional device.
- **Improved system performance** with higher speed than standard functions combined.



Notes

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